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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
JOHNSTON, PHILLIP A	

ART UNIT	PAPER NUMBER
2881	

DATE MAILED: 07/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/082,286	TAKANE ET AL.	
	Examiner	Art Unit	
	Phillip A Johnston	2881	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 May 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

1. This Office Action is submitted in response to Amendment dated 5-17-2004, wherein claims 1,24 and 25 have been amended. Claims 1-25 are pending.

Claims Rejection – 35 U.S.C. 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-25 stand rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,107,637 to Watanabe, in view of Okubo, U.S. Patent No. 5,872,862.

Watanabe (637) discloses that an object is inspected based on a two-dimensional SEM image obtained over a certain wide area. As a result, driving the beam deflector 102 to scan electron beams in the direction substantially perpendicular to the movement direction of the stage 105 while the stage 105 is being continuously moved, it is necessary to detect a two-dimensional secondary electron image signal by the secondary electron detector 104. Specifically, while the stage 105 is being

continuously moved in the X direction, for example, the beam deflector 102 is moved to scan electron beams in the Y direction substantially perpendicular to the movement direction of the stage 105, and then the stage 105 is moved in a stepwise fashion in the Y direction. Thereafter, while the stage 105 is being continuously moved in the X direction, the beam deflector 102 is driven to scan electron beams in the Y direction substantially perpendicular to the movement direction of the stage 105, and a two-dimensional secondary electron image signal has to be detected by the secondary electron detector 104. The processes of (1) continuous movement of the stage, (2) beam scanning, (3) optical height detection, (4) focus control and/or deflection direction and width correction, and (5) secondary electron image acquisition should be executed simultaneously. In this way, the acquired SEM image is kept focused and distortion-corrected while the image is being acquired continuously and speedily. By this control, fast and high-sensitivity defect detection can be achieved. Then, the image processing circuit 124 compares corresponding images or repetitive patterns by comparing an electron beam image delayed by the image memory and an image directly inputted from the A/D converter 124, thereby resulting in the comparison inspection being realized. The entirety control unit 120 receives the inspected result at the same time it controls the image processing circuit 124, and then displays the inspected result on the display 143 or stores the same in the memory 142. See Column 18, line 4-39.

Watanabe (637) also discloses the inspected object 106, on semiconductor wafer 3, where are arrayed a number of chips 3a which form the same product finally as shown in FIG. 5(a). An inside pattern layout of the chip 3a comprises a memory mat portion 3c in which memory cells are regularly arranged at the same pitch in a two-dimensional fashion and a peripheral circuit portion 3b as shown by an enlarged view in FIG. 5(b). When the present invention is applied to the inspection of the pattern of this semiconductor wafer 3, a detected image at a certain chip (e.g. chip 3d) is memorized in advance, and then compared with a detected image of another chip (e.g. 3e) (hereinafter referred to as "chip comparison"). Alternatively, a detected image at a certain memory cell (e.g. memory cell 3f) is memorized in advance, and then compared with a detected image of other cell (e.g. cell 3g) (hereinafter referred to as "cell comparison") as shown in FIG. 5(c), thereby resulting in a defect being recognized. See Column 18, line 57-67; and Column 19, line 1-8.

Watanabe (637) further discloses that after the dark level correction (dark level is corrected on the basis of the detection signal 71 during the beam blanking period), the electron beam current fluctuation correction (beam current intensity is monitored and a signal is normalized by a beam current) and the shading correction (fluctuation of quantity of light at the beam scanning position is corrected) are effected on the digital image data (gradation image data) 71 obtained from the electric converter (light-receiving element) 25, the filtering processing is effected on the corrected digital image data (gradation image data) 80 by a Gaussian filter, a mean value filter or an edge-emphasizing filter in the filtering processing circuit 81, thereby resulting a digital

image signal 82 with an image quality being improved. If necessary, a distortion of an image is corrected. These pre-processings are executed in order to convert a detected image so as to become advantageous in the later defect judgment processing.

Although the delay circuit 41 formed of a shift register or the like delays the digital image signal 82 (gradation image signal) with an improved image quality from the pre-processing circuit 40 by a constant time, if a delay time is obtained from the entirety control unit 120 and set to a time during which the stage 2 is moved by a chip pitch amount (d1 in FIG. 5(a)), then a delayed signal g0 and a signal f0 which is not delayed become image signals obtained at the same position of the adjacent chips, thereby resulting in the aforementioned chip comparison inspection being realized. Alternatively, if the delay time is obtained from the entirety control unit 120 and set to a time during which the stage 2 is moved by a pitch amount (d2 in FIG. 5(c)) of the memory cell, then the delayed signal g0 and the signal f0, which is not delayed become image signals obtained at the same position of the adjacent memory cells, thereby resulting in the aforementioned cell comparison inspection being realized. As described above, the delay circuit 41 is able to select an arbitrary delay time by controlling a read-out pixel position based on information obtained from the entirety control unit 120. As described above, compared digital image signals (gradation image signals) f0 and g0 are outputted from the image output unit 140. Hereinafter, f0 will be referred to as a detection image and g0 will be referred to as a comparison image. Incidentally, as shown in FIG. 7, the comparison image signal f0 may be

stored in a first image memory unit 46 composed of a shift register and an image memory and the detection image signal f0 may be stored in a second image memory unit 47 composed of a shift register and an image memory. As described above, the first image memory unit 46 may comprise the delay circuit 41, and the second image memory unit 47 is not necessarily required. See Column 23, line 13-62.

It is implied herein that correction of positional displacement of a comparison or reference image g0 in accordance with Watanabe (637) is equivalent to correcting the portion of the image that corresponds to the template, as recited in Claims 1, 24, and 25.

Watanabe (637) still further discloses that the image processing unit 124 includes the pre-processing circuit 40, which outputs a detection image f0(x, y) expressed by a gradation value (light and shade value) with respect to a certain inspection area on the inspected object 106, and the delay circuit 41 outputs a comparison image (standard image: reference image) g0(x, y) expressed by a gradation value (light and shade value) with respect to a certain area on the inspected object 106 which becomes a standard to be compared.

The pixel unit position alignment unit 42 of image processing unit 124 displaces the position of comparison image, for example, in such a manner that the position displacement amount of the comparison image g0(x, y) relative to the above-mentioned detection image f0(x, y) falls in a range of from 0 to 1 pixel, in other words, the position at which a "matching degree" between f0(x, y) and g0(x, y) becomes maximum falls within a range of from 0 to 1 pixel. As a consequence, as shown in

FIGS. 6(a) and 6(b), for example, the detection image f0(x, y) and the comparison image g0(x, y) are aligned with an alignment accuracy of less than one pixel. See Column 24, line 1-21.

It is implied herein that memorizing the corrected image of a chip on a wafer in advance as a reference image and then comparing it to a detected image of another chip in accordance with Watanabe (637) is equivalent to re-registering the portion of the image that corresponds to the template each time a matching process is performed, as recited in Claims 1, 24, and 25.

It is also implied herein that imaging pixel data in accordance with Watanabe (637) is equivalent the use of bitmap data, as recited in Claims 4,7,8, and 11-15.

Watanabe (637) as applied above does not disclose the use of CAD data, as recited in Claims 1,4, and 5. However, Okubo (862) describes a pattern matching apparatus that scans a sample with a Scanning Electron Microscope (SEM) to form a secondary electron image of wiring patterns and matches those patterns with patterns prepared from CAD data. As the electron beam unit 110 scans the sample 112, where secondary electrons emitted from the sample are detected by detector 120, and the output is converted by image input unit 122 into a digital image stored in the SEM image frame memory 123. The digitized SEM image is then displayed on display unit 124. The data stored in SEM memory 123 are read and processed by a computer 125. CAD data storage 127 stores CAD data that provides photomask wiring patterns. Computer 125 reads the CAD data out of the CAD data storage 127 according to a specified range, determines magnification Ms of the secondary electron image, sets the magnification

Ms in the SEM deflection controller 121, determines a target position of stage 111, sets the target position in the stage controller 126, matches the secondary electron image with the CAD data, and determines a measuring point on the secondary electron image according to a measuring point specified on the CAD data. See column 8 line 1-19.

It is implied that the digital image in SEM image frame memory 123 of Okubo (862), is the electronic equivalent of a bitmap.

Therefore it would have been obvious to one of ordinary skill in the art that the defect inspection apparatus and method of Watanabe (637) can be modified to use the CAD data in accordance with Okubo (862), so that digital images of CAD data could also be compared to the secondary electron image from a Scanning Electron Microscope .

Examiners Response to Arguments

4. Applicant's arguments filed 5-17-2004 have been fully considered but they are not persuasive.

Argument 1

Applicant states that, "Both Watanabe and Okubo fail to teach or suggest the unique feature of the present invention that, by performing a pattern matching process between a line image, such as a bitmap, and a grayscale image, such as an SEM

image, an image suitable for pattern matching is obtained from the grayscale image and re-registered as the template."

The applicant is respectfully directed to Watanabe (637), Column 24, line 1-21, which states; the image processing unit 124 includes the pre-processing circuit 40, which outputs a detection image f0(x, y) expressed by a gradation value (light and shade value) with respect to a certain inspection area on the inspected object 106, and the delay circuit 41 outputs a comparison image (standard image: reference image) g0(x, y) expressed by a gradation value (light and shade value) with respect to a certain area on the inspected object 106 which becomes a standard to be compared.

The pixel unit position alignment unit 42 of image processing unit 124 displaces the position of comparison image, for example, in such a manner that the position displacement amount of the comparison image g0(x, y) relative to the above-mentioned detection image f0(x, y) falls in a range of from 0 to 1 pixel, in other words, the position at which a "matching degree" between f0(x, y) and g0(x, y) becomes maximum falls within a range of from 0 to 1 pixel. As a consequence, as shown in FIGS. 6(a) and 6(b), for example, the detection image f0(x, y) and the comparison image g0(x, y) are aligned with an alignment accuracy of less than one pixel.

The applicant is also respectfully directed to Okubo (862), Column 24, line 55-58, which states; The apparatus reads gray scale (black and white) image data D1 from the memory 502, quadratically differentiates the image data D1 by the Laplacian operation element 501, and detects edges according to the quadratically differentiated values.

As well as, Column 30, line 5-10, which states; In this way, the first to fourth image processing methods according to the fifth aspect of the present invention detect edges according to edge information as well as clearness information (gray scale changing ratio), correctly carry out the weighting process, and accurately correlate binary image patterns with reference patterns.

The examiner has interpreted from the Watanabe (637) and Okubo (862) references above that a comparison is made between gray scale SEM images and reference (CAD data based) images, and that the comparison image becomes the new standard image to be compared, which is equivalent to the matching process recited in claims 1,24 and 25.

Conclusion

5. The Amendment filed on 5-17-2004 under 37 CFR 1.131 has been considered but is ineffective to overcome the Watanabe (637) and Okubo (862) references.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

6. Any inquiry concerning this communication or earlier communications should be directed to Phillip Johnston whose telephone number is (571) 272-2475. The examiner can normally be reached on Monday-Friday from 7:30 am to 4:00 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiners supervisor John Lee can be reached at (571) 272-2477. The fax phone number for the organization where the application or proceeding is assigned is 703 872 9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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PJ
July 13, 2004